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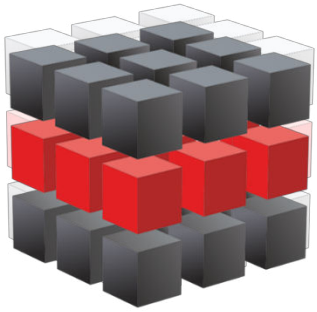

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CHENNAI – PONDICHERRY

VERY LARGE SCALE INTEGRATION 2019-2020

New Titles

1. Multistage Linear Feedback Shift Register Counters With Reduced Decoding Logic in 130-nm CMOS for Large-Scale Array Applications

Published in: IEEE Transactions on Very Large Scale Integration (VLSI) Systems (Volume: 27 , Issue: 1 , Jan. 2019)

2. Hybrid Logical Effort for Hybrid Logic Style Full Adders in Multistage Structures

Published in: IEEE Transactions on Very Large Scale Integration (VLSI) Systems (Volume: 27 , Issue: 5 , May 2019)

3. A 1.2-V 2.41-GHz Three-Stage CMOS OTA With Efficient Frequency Compensation Technique

Published in: IEEE Transactions on Circuits and Systems I: Regular Papers (Volume: 66 , Issue: 1 , Jan. 2019)

4. Robust Proportionate Adaptive Filter Architectures Under Impulsive Noise

Published in: IEEE Transactions on Very Large Scale Integration (VLSI) Systems (Volume: 27 , Issue: 5 , May 2019)

5. Dual-Channel Multiplier for Piecewise-Polynomial Function Evaluation for Low-Power 3-D Graphics

Published in: IEEE Transactions on Very Large Scale Integration (VLSI) Systems (Volume: 27 , Issue: 4 , April 2019)

6. A Two-Speed, Radix-4, Serial–Parallel Multiplier

Published in: IEEE Transactions on Very Large Scale Integration (VLSI) Systems (Volume: 27 , Issue: 4 , April 2019)

7. Designing Efficient Circuits Based on Runtime-Reconfigurable Field-Effect Transistors

Published in: IEEE Transactions on Very Large Scale Integration (VLSI) Systems (Volume: 27 , Issue: 3 , March 2019)

8. Three-Dimensional Monolithic FinFET-Based 8T SRAM Cell Design for Enhanced Read Time and Low Leakage

Published in: IEEE Transactions on Very Large Scale Integration (VLSI) Systems (Volume: 27 , Issue: 4 , April 2019)

9. Efficiently Mapping VLSI Circuits With Simple Cells

Published in: IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (Volume: 38 , Issue: 4 , April 2019)

10. A Carry Lookahead Adder Based on Hybrid CMOS-Memristor Logic Circuit

Published in: IEEE Access (Volume: 7)

11. Optimization Design on Active Guard Ring to Improve Latch-Up Immunity of CMOS Integrated Circuits

Published in: IEEE Transactions on Electron Devices (Volume: 66 , Issue: 4 , April 2019)

12. A 7T-SRAM With Data-Write Technique by Capacitive Coupling

Published in: IEEE Journal of Solid-State Circuits (Volume: 54 , Issue: 2 , Feb. 2019)

13. Adaptively Biased Output Cap-Less NMOS LDO With 19 ns Settling Time

Published in: IEEE Transactions on Circuits and Systems II: Express Briefs (Volume: 66 , Issue: 2 , Feb. 2019)

14. A 60GHz CMOS Power Amplifier with Parametric Matching Networks-(ADS Software)

Published in: 2019 IEEE Texas Symposium on Wireless and Microwave Circuits and Systems (WMCS)

15. A CMOS PUF Circuit Primitive Based on a Two-Dimensional Nonlinear Dynamical System -(ADS Software)

Published in: 2019 IEEE International Symposium on Circuits and Systems (ISCAS)

16. A Digital-to-Time Converter with Coupled Phase- Rotating LC Oscillators in 90-nm CMOS Technology-(ADS Software)

Published in: 2019 IEEE International Symposium on Circuits and Systems (ISCAS)

17. A Low Noise Fault Tolerant Radiation Hardened 2.56 Gbps Clock-Data Recovery Circuit with High Speed Feed Forward Correction in 65 nm CMOS. -(ADS Software)

Published in: 2019 IEEE 10th Latin American Symposium on Circuits & Systems (LASCAS)

18. CMOS implementation of wide frequency bandwidth Resonator's Q-factor measurement circuit.

Published in: 2019 IEEE International Symposium on Circuits and Systems (ISCAS)

19. Design of Low Leakage SRAM Bitcell

Published in: 2019 IEEE 39th International Conference on Electronics and Nanotechnology (ELNANO)