Medium Access Control in Wireless Network-on-Chip: A Context Analysis

ABSTRACT

- Wireless on-chip communication is a promising candidate to address the performance and efficiency issues that arise when scaling current NoC techniques to manycore processors. A WNoC can serve global and broadcast trafc with ultra-low latency even in thousand-core chips, thus acting as a natural complement to conventional and throughput-oriented wireline NoCs. However, the development of MAC strategies needed to efficiently share the wireless medium among the increasing number of cores remains a considerable challenge given the singularities of the environment and the novelty of the research area. In this position article, we present a context analysis describing the physical constraints, performance objectives, and trafc characteristics of the on-chip communication paradigm.

EXISTING SYSTEM

- The relentless march of technology scaling has forced a widespread transition in processor design from *single-core* to *multicore* due to power and complexity reasons. After this paradigm shift, successive generations of processors have changed the way to achieve higher performance from increasing the operation frequency to integrating more cores within the same chip.

PROPOSED SYSTEM

- we present a context analysis describing the physical constraints, performance objectives, and trafc characteristics of the on-chip communication paradigm. We summarize the main differences with respect to traditional wireless scenarios, and then discuss their implications on the design of MAC protocols for manycore WNoC, with the ultimate goal of kickstarting this arguably unexplored research area.

CONTINUE

- Wireless on-chip communication, enabled by recent advances in integrated RF design, is among the considered alternatives given its multiple advantages:
- Low latency for communications between distant cores by virtue of speed-of-light propagation Natural broadcast capabilities via omnidirectional radiation.
- System-level flexibility and non-intrusiveness given by the lack of additional wires between cores.
- Compatibility with complementary metal oxide semiconductor (CMOS) and reuse of knowledge gained in other wireless scenarios.

HARDWARE REQUIREMENTS

- Processor - Pentium –III
- Speed - 1.1 Ghz
- RAM - 256 MB(min)
- Hard Disk - 20 GB
- Floppy Drive - 1.44 MB
- Key Board - Standard Windows Keyboard
- Mouse - Two or Three Button Mouse
- Monitor - SVGA

SOFTWARE REQUIREMENTS

- Operating System : Windows 8
- Front End : Java /DOTNET
- Database : Mysql/HEIDISQL

CONCLUSION

- With the potential to off er low-power and low-latency global and broadcast communication, wireless on-chip communication holds great promise for the implementation of NoCs for manycore chips. However, it is necessary to develop scalable, fast, and efficient MAC mechanisms to exploit such potential. This position article has provided a rigorous context analysis with the aim to clarify the singularities of this new environment for MAC protocol research, which features both very stringent requirements and unique optimization opportunities. On one hand, the analysis highlights latency, reliability, and variability of trafc as the most challenging aspects of the scenario; on the other hand, the analysis points to the static, controlled, and monolithic nature of a multiprocessor as the most salient characteristics potentially leading to unprecedented performance via cross-layer design far beyond traditional limits.

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