A TEST SELECTION PROCEDURE FOR IMPROVING THE ACCURACY OF DEFECT DIAGNOSIS

ABSTRACT

• The premise behind these procedures is that most of the tests in a given test set are useful for defect diagnosis, and only small numbers of tests need to be ignored.

• This paper makes the new observation that it is possible to use small subsets of tests to obtain more accurate diagnosis results.

• This paper describes a procedure that starts from an empty test set, and adds tests one at a time. The test selected at every iteration is the one that results in the smallest candidate fault set.

• The addition of tests increases the number of candidate faults gradually. Experimental results for benchmark circuits demonstrate that the addition of tests provides more candidate fault sets with higher degrees of accuracy than the removal of tests. One of these candidate fault sets can be used for failure analysis.

EXISTING SYSTEM

• Experimental results also indicate that a defect diagnosis procedure does not require the complete observed response of a faulty chip in order to produce accurate diagnosis results.
• Motivated by these observations, this paper augments a defect diagnosis procedure with a process that removes from consideration tests whose effects on the results of diagnosis may be negative.

• The augmented procedure runs the underlying defect diagnosis procedure several times in order to decide which tests should be removed from consideration.

• Experimental results indicate that this results in smaller sets of candidate faults and improved accuracy of diagnosis.

PROPOSED SYSTEM

• The procedure starts from an empty test set, and adds tests one at a time so as to obtain the smallest possible candidate fault sets.

• The procedure computes candidate fault sets that are all contained in the basic set, which is obtained using the entire test set.

• This ensures that the candidate fault sets will not contain unnecessary candidate faults, and contributes to the accuracy of defect diagnosis.

• The experimental results for benchmark circuits demonstrated that smaller test sets yield smaller candidate fault sets that are more accurate than the sets obtained with the entire test set, or by ignoring small numbers of tests.

HARDWARE REQUIREMENTS

• Processor - Pentium-IV
8+ Years of Excellence in IEEE Project development for universities across INDIA, USA, UK, AUSTRALIA, SWEDEN.
Expert developers in JAVA, DOT NET, ANDROID, PHP, MATLAB, NS2, NS3, VLSI, CLOUD SIM, TANNER, MICROWIND, EMBEDDED, ROBOTICS, MECHANICAL, MECHATRONICS, WIRELESS NETWORKS, OPNET, OMNET.
Over 11000+ projects, 425 clients - MICANS INFOTECH provides IEEE & application projects for CSE, IT, ECE, EEE, MECH, CIVIL, MCA, M.TECH, M.PHILL, MBA, DME, MS, PHD.

Projects with FUTURE WORK / LIVE DEVELOPMENT / FACE TO FACE CLASSES
ONLY PROJECT CENTER WITH OWN DEVELOPERS - CSE, IT, ECE, MECH, CIVIL, EEE

PONDICHERRY – VILLUPURAM – CHENNAI - HYDERABAD

- Speed - 1.1 Ghz
- RAM - 256MB (min)
- Hard Disk - 20 GB
- Key Board - Standard Windows Keyboard
- Mouse - Two or Three Button Mouse
- Monitor - SVGA

SOFTWARE REQUIREMENTS
- Tool - Network Simulator 2
- Operating system - LINUX
- Front end - OTCL (Object Oriented Tool Command Language)

REFERENCES
MICANS INFOTECH

+91 90036 28940 +91 94435 11725

- 8+ Years of Excellence in IEEE Project development for universities across INDIA, USA, UK, AUSTRALIA, SWEDEN.
- Expert developers in JAVA, DOT NET, ANDROID, PHP, MATLAB, NS2, NS3, VLSI, CLOUD SIM, TANNER, MICROWIND, EMBEDDED, ROBOTICS, MECHANICAL, MECHATRONICS, WIRELESS NETWORKS, OPNET, OMNET
- Over 11000+ projects, 425 clients - MICANS INFOTECH provides IEEE & application projects for CSE, IT, ECE, EEE, MECH, CIVIL, MCA, M.TECH, M.PHILL, MBA, DME, MS, PHD.

Projects with FUTURE WORK / LIVE DEVELOPMENT / FACE TO FACE CLASSES
ONLY PROJECT CENTER WITH OWN DEVELOPERS - CSE, IT, ECE, MECH, CIVIL, EEE

PONDICHERRY – VILLUPURAM – CHENNAI - HYDERABAD