A COMPACT ONE-PIN MODE TRANSITION CIRCUIT FOR CLOCK SYNCHRONIZATION IN CURRENT-MODE-CONTROLLED SWITCHING REGULATORS

ABSTRACT

- The proposed circuit reduces the circuit complexity needed to achieve mode transition during synchronization by utilizing switched-capacitor and sampling design techniques.

- It linearly converts the input clock frequency to a current to maintain constant amount of slope compensation for current-mode switching regulators across their switching frequency range of operation.

- This circuit is designed to operate from 100 KHz to 2.5 MHz and fabricated in a 0.35-µm BiCMOS–DMOS process. The total solution occupies 0.082 mm² die area.

- Experimental results are presented from peak-current-mode buck regulators with one-pin synchronization circuit to show the performance improvement of using the proposed design approach over a phase-locked-loop-based design.

EXISTING SYSTEM

- This paper reports a delay locked loop (DLL) based hysteretic controller for high-frequency multiphase buck DC-DC converters.

- The DLL control loop employs the switching frequency from a hysteretic comparator to automatically synchronize the remaining phases.
• A dedicated duty cycle control loop is used to enable current sharing and ripple cancellation.

• We demonstrate a 25-70 MHz 4-phase converter with fast hysteretic control and output conversion range of 17%-80% while achieving a peak efficiency of 83% and peak-to-peak ripple within 10% in standard 0.6 mm 5 V CMOS process.

PROPOSED SYSTEM

• A compact implementation of one-pin mode transition circuit that can circumvent the issues related to the mode transitions between external resistor and external clock is presented.

• The simplicity and small size of the proposed design allow for its integration with switching regulators to make them immune to RT and CLK mode transitions.

• The advantages of the proposed design are demonstrated by employing this circuit in a peak-current-mode-controlled switching regulator and comparing its response with another switching regulator using a PLL-based synchronization circuit.

• The proposed circuit helps synchronizing the switch regulator and maintaining its output during these transitions. This feature becomes especially useful for the clock synchronization of switch regulators in applications, such as multi rail systems.

HARDWARE REQUIREMENTS

• Processor - Pentium-IV
• Speed - 1.1 Ghz
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Expert developers in JAVA, DOT NET, ANDROID, PHP, MATLAB, NS2, NS3, VLSI, CLOUD SIM, TANNER, MICROWIND, EMBEDDED, ROBOTICS, MECHANICAL, MECHATRONICS, WIRELESS NETWORKS, OPNET, OMNET
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• RAM - 256MB (min)
• Hard Disk - 20 GB
• Key Board - Standard Windows Keyboard
• Mouse - Two or Three Button Mouse
• Monitor - SVGA

SOFTWARE REQUIREMENTS

• Tool - Network Simulator-2
• Operating system - LINUX
• Front end - OTCL (Object Oriented Tool Command Language)

REFERENCES

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- Expert developers in JAVA, DOT NET, ANDROID, PHP, MATLAB, NS2, NS3, VLSI, CLOUD SIM, TANNER, MICROWIND, EMBEDDED, ROBOTICS, MECHANICAL, MECHATRONICS, WIRELESS NETWORKS, OPNET, OMNET

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